SUB D2

48. (Second Amended) A capacitor comprising:

C2

a material layer having a first level and a second level, said first and second levels being connected by a sidewall region between said first and second levels;

a doped BST high dielectric constant thin film material deposited on at least one said sidewall region, said deposited BST thin film material having a post deposition doping such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a capping layer provided over at least a portion of said BST thin film material.

SUB D3

74. (Second Amended) An integrated circuit capacitor device comprising:

C3

a material layer having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided at least on said sidewall region;

a doped BST high dielectric constant thin film material provided on at least one said first electrode, said deposited BST high dielectric thin film material having a post deposition doping such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a second electrode provided on said BST high dielectric thin film layer.

REMARKS/ARGUMENTS

Claims 39, 41-48, 51-56, and 74-83 are pending in this application. Attached hereto is a marked up version of the changes made to claims 39, 48 and 74 by the current amendment. The attached page is captioned **"Version with markings to show changes made."**